UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,516	07/10/2007	Jochen Kuehner	10191/4807	1707

26646 7590 03/11/2008

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
WELLS, KENNETH B	
ART UNIT	PAPER NUMBER
2816	
MAIL DATE	DELIVERY MODE
03/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,516	KUEHNER ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 9/19/06 has been considered by the examiner.

Specification

2. The disclosure is objected to because of the following informalities: on page 2, lines 9-10, reference to claims 1 and 16 should be deleted because these claims are no longer pending. On page 8, line 7, it appears that "switched-on" (second occurrence) should be changed to --switched off--.

Appropriate correction is required.

Drawings

3. The drawings are objected to because Figs. 1 and 2 need "prior art" labels. Also in Fig. 1, diode "D" should be changed to --DA-- so as to be consistent with the specification (note the same problem in Fig. 2). Also in Fig. 1, the black box receiving signal Vx needs a text label (note the same problem in Fig. 3 with regard to

circuits 10 and 12, and also Fig. 6 with regard to circuits 20 through 25). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. Claims 23-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It cannot be determined what is meant by "self-blocking" or "self-conducting" as it pertains to semiconductor switches (i.e., this is not a common term of art and applicant should therefore define these terms so that it can be understood what is meant here).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 17-19 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchida et al.

As to claim 17, note Figs. 7 and 8, where the recited "semiconductor switch" reads on switch 101; the recited "line" reads on the wire between switch 101 and load element 102 (which reads on the recited "component in the current path"); the recited "controllable current source" reads on either variable current source 131 or 132 shown in Fig. 8; and the recited "control unit" reads on either logic circuitry 104 by itself or in combination with the feedback circuitry between the source of transistor 101 and the inputs of logic circuitry 104. Note also that the variable current sources are controlled by the output from logic circuitry 104 during switching operation of switch 101, and the circuit functions to prevent and over voltage from occurring across the drain and source terminals of switch 101. The recited "set point terminal voltage" reads on either of the fixed the voltages set by voltage sources 115 and 116.

As to claim 18, the values selected for voltage sources 115 and 116 are determined based on the maximum permissible terminal voltage between the drain and source of switch 101.

As to claim 19, the recited in comparator reads on any one of comparator circuits 106, 112 and 114.

As to claim 32, this claim is rejected using the same analysis as set forth above with regard to claim 17.

6. Claims 17-19 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Glogolja.

As to claim 17, note Fig. 4, where the recited "semiconductor switch" reads on switch 13; the recited "line" reads on the wire between switch 13 and inductors 23 and 25 (either of which reads on the recited "component in the current path"); the recited "controllable current source" reads on BJT 55 (or, alternatively, either of transistors 51 and 53); and the recited "control unit" reads on either monitor circuit 49, monitor circuit 47 or controller 43 (or any combination of these three circuits). Note also that the circuit functions to prevent and over voltage from occurring across the collector and emitter terminals of switch 13. The recited "set point terminal voltage" is set inside controller 43.

As to claim 18, the value of the set point voltage is determined based on the maximum permissible terminal voltage between the collector and emitter of switch 13.

As to claim 19, the recited in comparator is inside monitor circuit 49 or monitor circuit 47 (these circuits inherently must have some comparator circuitry in order to detect the level of the current flowing through transistor 13).

As to claim 32, this claim is rejected using the same analysis as set forth above with regard to claim 17.

7. Claims 17-19, 31 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Tai.

As to claim 17, note Fig. 2 ofthe recited "semiconductor switch" reads on switch 9; the recited "line" reads on either of the wires connected to the collector and emitter of switch 9; the recited "controllable current source" reads on current source 6; and the recited "control unit" reads on the combination of circuits 3, 4, 5 and 7). Note also that the circuit functions to prevent an over voltage from occurring across the collector and emitter terminals of switch 9. The recited "set point terminal voltage" is set by circuit 4.

As to claim 18, the value of the set point voltage is determined based on the maximum permissible terminal

voltage between the collector and emitter of switch 9.

As to claim 19, the recited in comparator reads on circuit 5.

As to claim 31, note that switch 9 is an IGBT.

As to claim 32, this claim is rejected using the same analysis as set forth above with regard to claim 17.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Tsuchida et al, Glogolja and Tai in view of Akagai et al.

The recited P controller, though not disclosed, nevertheless would have been obvious to any person having ordinary skill in the art at the time of applicant's invention because control units having proportional type controllers are old and well-known in the art, one example

of this being disclosed by Akagai et al (note PI controllers 21 and 31 which are used in an over voltage protection circuit in a feedback loop thereof). The motivation for using such a PI controller and the over voltage protection circuits of the above-noted primary references is to achieve the well-known advantages that are obtained from using such well-known control circuits. Thus, claim 20 does not distinguish patentably over any one of Tsuchida et al, Glogolja and Tai in view of Akagai et al.

9. Claims 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Tsuchida et al, Glogolja and Tai.

As to claim 21, although these references do not state that the voltage across the semiconductor switch rises above the operating voltage, such would have been obvious to any person having ordinary skill in the art at the time of applicant's invention because it is old and well-known in the art that over voltages often rise above the level of Vcc due to, inter alia, noise spikes and other transient voltage conditions, of which fact official notice is taken by the examiner.

As to claim 22, note that in each of the above-noted references, during operation of the circuits, there will inherently be a point in time where the voltage at the control input of the semiconductor switch that is lower than the potential at either of the main current carrying terminals of the semiconductor switch (where the recited current path is between these main current carrying terminals). For example, note that the base terminal of transistor 13 in Glogolja will be biased to potential -V2 when transistor 53 is in a saturated state, and also note that the drain and source of transistor 101 in Tsuchida et al will have relatively high potential values because it is used as a high side switch. The same also appears to be the case during the operation of Tai's over voltage protection circuitry.

As to claims 23 and 24, to the extent understood, these claim limitations also would have been obvious because it is also old and well-known in the art to adjust a set point terminal voltage during operation of an over voltage protection circuit, note each of the references listed in paragraph ten below.

As to claims 25-27, the use of delay and timing elements in over voltage protection circuits is also old

and well-known in the art, again note the references listed in paragraph ten below.

As to claims 28-30, official notice is taken that it is well-known in the art of self-commutated inverters to control the amount of delay in the on/off control of the individual semiconductor switches, and thus these claims similarly do not distinguish patentably over the above-noted prior art.

Other Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note that the use of adjusting a setpoint terminal voltage in over voltage protection circuits taught by DePuy, Rogowsky, Ma et al, Chacon, Kanouda et al, Mutoh et al, Steinshorn and Zimmerman. Also note the use of timing and delay circuits in over voltage protection circuits disclosed by Mutoh et al and Cawley et al. Finally, note Fig. 1 of Schoofs et al and Fig. 3 of Mizuno et al, each of which is also seen to anticipate at least claims 17 and 32 under 35 U.S.C. 102(b).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards, can be reached at (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816

March 3, 2008